APPLICATION NOTE 41

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1.0 INTRODUCTION

PWM applications are complex systems with a highly non-linear modulation/demodulation system at the heart of things. This mandates a collection of poles and zeros plus high harmonic and sub-harmonic content. This is further complicated by the fact that gain of the PWM block varies with supply voltage. These factors can make stability considerations a confusing issue without a plan of attack, that includes test criteria and some tools to obtain data. The successful design will arrange all the break points in a manner to avoid oscillation while maximizing bandwidth.

2.0 THE BASIC SYSTEM AND ITS CHALLENGES

Refer to Figure 1 showing the basic elements of a PWM amplifier circuit. The integrator will drive the PWM block where ever required to force feedback current to be equal and opposite of the input current. We will discuss only analog implementations, but computerized systems will function in a similar fashion. The PWM block translates its input to time modulated pulses of full supply amplitude. As of May 2001, all Apex PWM full-bridge amplifiers utilize locked anti-phase modulation (when one output is high, the other is always low; 50% modulation means equal times high and low for each cycle of switching frequency and after demodulation, 0V at the load). For more detail, see APPLICATION NOTE 30, PWM BASICS. The low pass power filter demodulates the PWM signal so the load sees little of the switching frequency carrier. It is in these modulation and demodulation stages that signal and carrier frequencies are mixed, as well as sums and differences are generated. The low pass signal filter has multiple input connection options; however, in all options, it reduces the carrier content that the feedback gain amplifier must deal with.

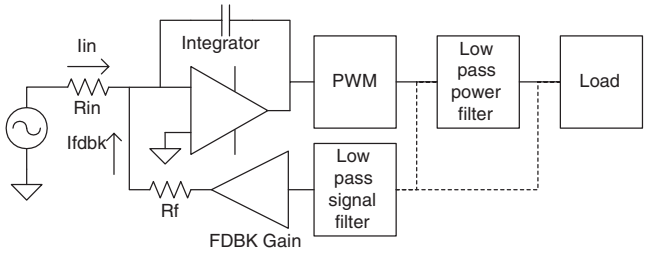


FIGURE 1. A TYPICAL PWM SYSTEM

Notice that the low pass function in the feedback loop will tend to make closed loop gain of the total system INCREASE above its corner frequency. Or we could say the pole in the feedback loop is going to cause the same stability problem as a zero in the closed loop gain of the system. To better understand the system, we will examine the various poles and zeros plus other problem areas.

Knowing the gain of the PWM block will be critical to analyzing this system. Finding the exact gain of the PWM block, including the effects of dead time, internal voltage loss and reverse currents in the catch diodes would be a formidable task. A suitable approximation is to compare full scale input with ideal full scale output. Product data sheets will give analog input voltages needed to generate modulation percentages. Modulation extremes will correspond to the upper and lower peaks of the ramp. Full scale input is then = VRAMPp-p. Full scale output on a single pin is the voltage change from 0 to 100% modulation, which equals supply voltage. In the case of a full bridge, we need to multiply this by two, because the load is connected differentially, seeing two equal and opposite drive voltages.

Gain of the PWM block = Vout p-p / Vramp p-p (1)

Where Vout p-p = Vs for half bridges and Vs * 2 for full bridges and Vramp p-p is set by the specific amplifier model, generally between 2.5 and 5V p-p. A full bridge PWM with a 4V ramp, running on 40V, has a gain of 20.

As the ratio between ramp voltage and supply voltage increases, the gain increases. Note that some PWM amplifiers, such as the SA50 and SA60, vary the modulation ramp voltage as Vcc varies. It would be acceptable to think of this changing gain as a changing gain-bandwidth product in an op amp circuit. The integrator and the PWM block are in series, so when viewed together, the gains of the two stages are added. Just as in linear circuits, achieving stable operation will be easier when all gain blocks are low compared to a system having higher gain blocks. In all cases, phase margin of the circuit will decrease as PWM gain increases. This means stability must be checked at maximum Vs, and minimum Vcc if appropriate. On the other side of the coin, check bandwidth at minimum Vs and maximum Vcc.

The job of the power filter is to attenuate the square, time modulated carrier and deliver only (ideally) the low frequency signal to the load. If the filter does a very good job, feedback must be taken ahead of the filter. If the filter is designed to have a minimum effect, feedback may be taken after the filter. In either case, the feedback signal will contain significant amounts of high frequency energy.

Taking voltage feedback after the power filter can put a PWM circuit well on the way to being a power oscillator. These filters contain a minimum of one series inductor and often some large capacitors on the load side of the inductor(s). If the filter design is not proper, or the load impedance has shifted after the filter was designed, the series L-C section(s) of the filter can produce serious peaking at the output. Even properly designed and terminated filters produce wild phase shift near their cutoff frequency. The technique of taking voltage feedback after the power filter is usually reserved for very special cases, the filter will be first order (inductor only) and the load is doing most of the filtering.

The low pass signal filter is used to attenuate the high frequency content of square PWM wave forms which have very short rise and fall times. Without this roll off, feedback gain amplifiers would need unrealistic bandwidth capability. The down side here is that a pole in the feedback path equates to a zero in the closed loop gain, a red flag for possible stability concerns.

Even with this filter, op amps picked for this job should exhibit superior high frequency common mode rejection. The non-linear response of feedback amplifiers can add extraneous signals to the feedback. The problem comes from the fact that feeding an op amp signals well above its bandwidth capability will often force the input stage into non-linear operation, resulting in what appears to be an offset error. This is compounded by the fact

the high frequency content (spikes) of PWM signals varies with modulation percentage. Imagine trying to drive a sine wave when an extra pulse is inserted every cycle between 150° and 180° and again between 330° and 360°! This is a path to distortion and in severe cases, to oscillation.

Along with R_F, the feedback voltage provides current to charge the integrator capacitor to the proper level. This capacitor should be the dominant frequency limiting element of the entire system. So, just where is the pole created by the integrator capacitor? As there is no resistor directly in parallel with this capacitor, the traditional calculation for an op amp roll off capacitor will not work. However, if such a resistor were in place (rather than our complex feedback loop), what would its value be? This fictitious value would result in the same change of integrator output voltage for a given change of input voltage, as occurs in the real system. To re-phrase, if we know Δinput current to the integrator, and output voltage of the integrator, then Ohms law dictates the effective feedback resistance must be ΔVOUT/ΔIIN. To answer these questions we need to know the input signal, the input resistor and how much the output of the integrator will move in response to the input signal.

To find this fictitious feedback resistor, refer to Figure 2, and assume a convenient input and use the given transfer function to find the PWM output voltage. Now divide by PWM gain (equation 1) to find the movement of the integrator voltage.

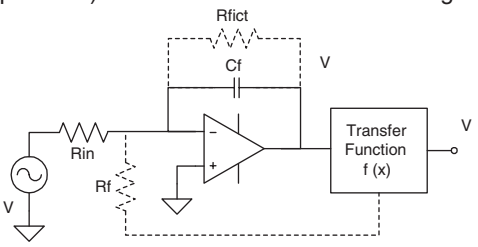


FIGURE 2. REPLACING THE REAL FEEDBACK SYSTEM WITH A FICTITIOUS RESISTOR

$$R_{FICTITIOUS} = R_{IN} * \Delta integrator / \Delta input \quad (2)$$

Using this fictitious feedback resistor, the pole frequency can be calculated just as if it were an op amp with parallel R-C feedback. When powering the SA01 (full-bridge and 5V p-p ramp) on 75V, gain of the PWM block is 30. If the circuit is configured for a gain of 10 (say, ±5Vin, ±50Vout) and the input resistor is 5K, Δ out =100, Δ integrator =3.333, Δinput = 10, and Δthe fictitious resistor is 1.67K. Even though the real RF maybe 5KΩ, a 0.1μF capacitor produces a pole at 953Hz.

If the overall system is controlling current rather than voltage, the foregoing is still true, and we have a new concern. The load is always inside the feedback loop for current control. Given a constant output current, output voltage will be a function of load impedance. This also means that load impedance is a factor in the integrator output swing, thus affecting the value of our fictitious feedback resistor, the pole frequency set with the integrating capacitor, system bandwidth, and stability. If load impedance changes only with factors other than frequency, such as resistor element thermal variation, the circuit can usually be checked at the two extremes and no special measures are required.

More often the load contains significant inductance which demands output voltage increase with frequency and it adds the V-to-I phase shift of the inductor to the feedback loop. In these cases, an additional voltage feedback path is usually added. The objective is to have this path come into play at a low enough frequency to avoid a stability problem, but high enough to achieve desired bandwidth.

The most common topology for current control is to use a differential amplifier, monitoring sense resistors in both the lower legs of the H-bridge. This leads to non-textbook filter design for current output circuits, especially when the load is inductive. This current sense yields a combination of load current, matching network current, plus filter capacitor current. To minimize errors in the load current, the filter and matching network need to be very light handed in the input signal frequency band. Filters will often be first order and matching network impedance will be increased as high as voltage peaking concerns will allow.

Servo loops are even more complex in that feedback is usually taken from position or velocity sensors. In these cases, power filtering is at an absolute minimum and additional compensation networks are sometimes applied with or between sensors, signal conditioners and the integrator.

Before proceeding, lets take notice of two items not included in this list of problem areas: frequency domain performance of the PWM block and the op amps used for feedback gain and for the integrator. With the frequency relationships discussed below, it can be demonstrated how the PWM block response is an insignificant problem. Op amps selected to meet the common mode rejection requirement at FSW, will automatically have enough gain-bandwidth product to not cause problems at the lower frequencies to be amplified.

3.0 FREQUENCY RELATIONSHIPS

The PWM F_{SW}, and required attenuation of F_{SW} at the load limit power filter the cutoff frequency, F_C. A reasonable starting place is to allow at least a decade between these two frequencies. A second way to look at this is to say you will allow at least ten segments or pulses to approximate the waveform delivered to the load. If the load is sensitive to high frequency components in the drive voltage, a larger ratio between these two frequencies will help and adding more poles to the filter will help. See APPLICATION NOTE 32 PWM LOW PASS FILTERING for additional information.

The low pass signal filter consists of one or more R-C pairs. The corner frequency is usually a decade or more below F_{SW}. The common mode capability of op amps, Vs , and system bandwidth requirements all factor into the design. If feedback is taken directly at the PWM output (by far the most common method), this filter sees a square wave input with peak-to-peak amplitude nearly equal to Vs. If feedback is taken after the power filter, phase shift of the power filter is added to the loop response. For this reason, a power filter inside the loop will be low Q and low attenuation.

The integrator pole frequency will be a fraction of the feedback pole(s). The higher the supply voltage, the smaller the fraction that should be used.

4.0 THE TECHNIQUE: PLOT 1/SSETA AVOID PEAKING

While the final filtered output is the objective of the PWM application, the best observation point is the integrator output. This approach allows borrowing some software analysis techniques from the op amp world. Even in the hardware world, it is often easier to monitor the integrator output (non switching and usually in the range of 0 to 10V) than monitor the output (switching, often differential, and centered at half the supply voltage).

The process of calculating the feedback factor of the integrator is similar to that for a more traditional op amp circuit. First, assign a value of 1V to the integrator swing, and then calculate through all feedback paths back to the input(s). To

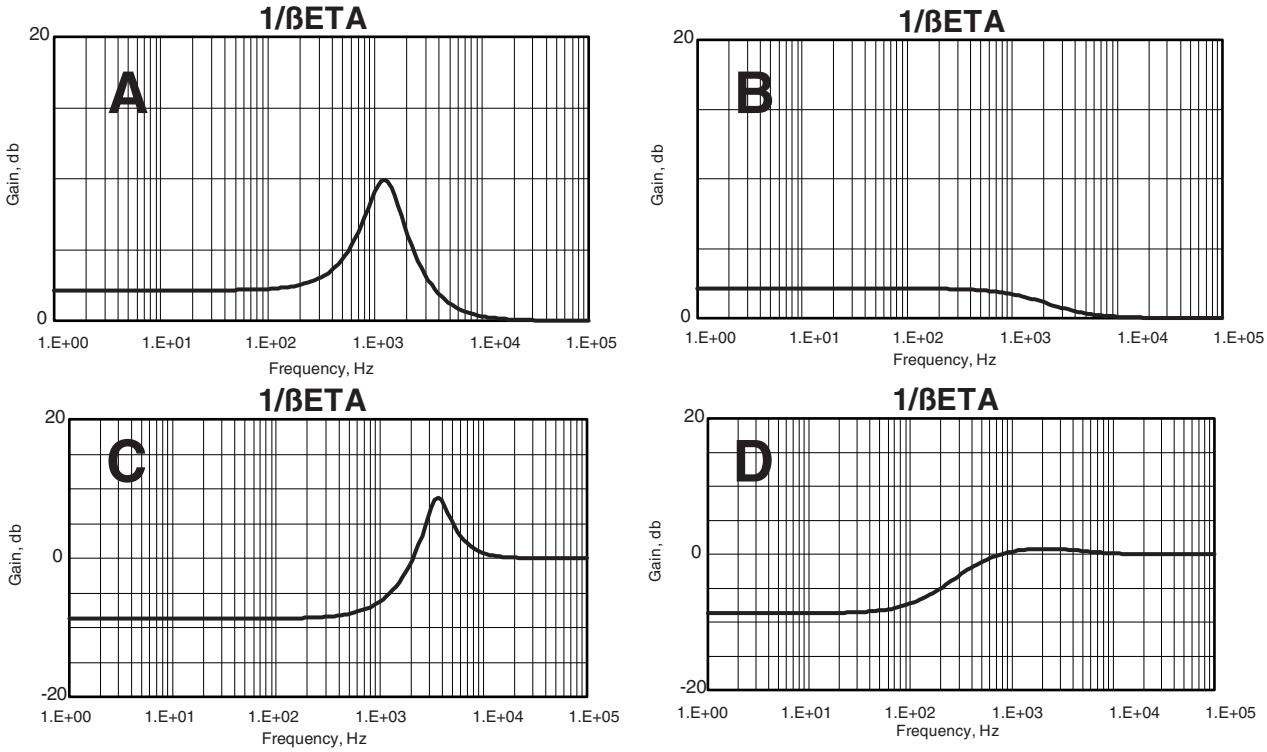


FIGURE 3. BASIC POSSIBILITIES FOR SHAPE OF THE 1/ßETA CURVE

finish the job, combine positive feedback (if it exists) with the negative; invert the feedback factor to obtain 1/ßeta, convert to dB, and plot the results. The objective will be to minimize or avoid peaking in this curve to assure a stable circuit.

There is one major point we learned for op amps that we must discard: "Feedback factor is always between 0 and 1, meaning feedback is limited from nothing to 100%". Because the PWM circuit has a gain block between the integrator and the feedback, it is possible to feed back more than 100% at low frequencies! At high frequencies, the integrator capacitors force 1/ßeta to 0dB, meaning there will be an increase in 1ßeta.

Refer to Figure 3 for examples of both peaking and non-peaking performance. Plot A resembles an op amp circuit with problems; low frequency 1/ßeta is positive, the peak spells trouble, and 0dB is approached at high frequency. Plot B is more what we want to see to insure stability. If bandwidth is not a concern, no peaking is desirable. When speed is a significant concern, some peaking will help, but at the expense of phase margin. For this case, peaking is defined as rise above the low frequency value.

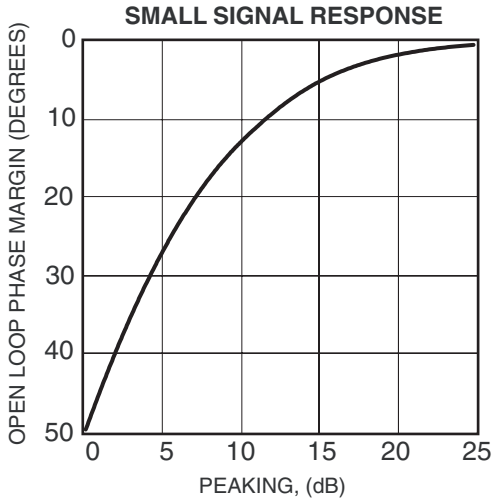


FIGURE 4. CONVERTING SYSTEM RESPONSE TO PHASE MARGIN

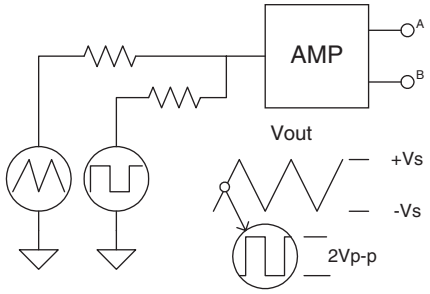
Plots C and D are again bad and good, except for the case where low frequency 1/ßeta is negative. This will occur more often with the higher voltage amplifiers and it will be more difficult to eliminate all peaking without a severe penalty in bandwidth. The rise from the initial negative value to 0dB at high frequency is not part of the peaking we are looking for. For this case, peaking is defined as just the rise above 0dB.

Judgment criteria for PWM circuit stability will be taken from hardware tests often used in the linear world. The system response peaking curve as shown in Figure 4 is the first criteria used. This test can be applied to the 1/ßeta curve mentioned earlier, to Spice simulations, or to actual hardware. With the system running closed loop, plot the frequency response of the integrator output. Then extract the amount of peaking, using the above definitions. Note that this test is not defined over 50°.

The square wave peaking test as shown in Figure 5 (next page) can be applied to either Spice simulations or to hardware. Sum two input signals to produce a small square wave riding on a much slower triangle (or sine). If a nominal 2Vp-p square wave displays a step peaking at 2.5V, phase margin is about 35°.

5.0 GENERAL TOPOLOGY SELECTION

Figure 6 (next page) illustrates the two most common topologies for controlling output voltage. While the filter and load are part of the system, they are outside the feedback loop in most voltage control systems and can be ignored for the most basic analysis. Type V1 requires an additional amplifier, but this topology lends itself well to level shifting input signals (unipolar input producing bipolar output) with a single resistor because the summing junction does not move as the input signal varies.



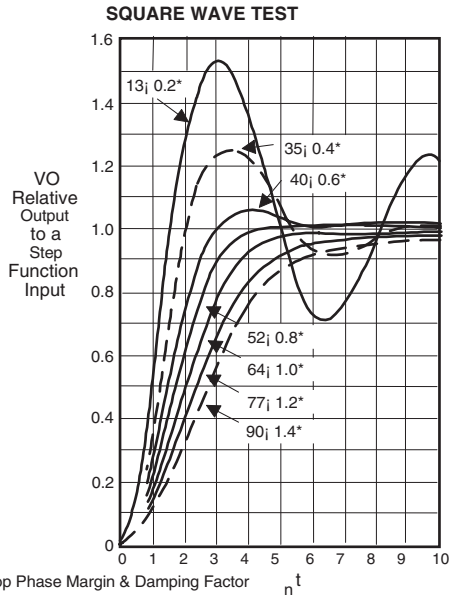


FIGURE 5. THE SQUARE WAVE STABILITY TEST AND RESULTS INTERPRETATION

Type V2 is simpler, but does not go well with single resistor level shifting because the summing junction moves as the input signal varies. To level the shift, a reference capable of sinking and sourcing current should be applied to the opposite input signal location. This circuit then functions similar to a four resistor difference amplifier, except a T-network of two resistors and a capacitor replaces each single R_F (add the two resistors for DC gain calculations), and the pin normally labeled reference is connected to the inverting PWM output. The output is now differential rather than single ended and DC circuit gain is simply R_{Ftotal}/R_{IN}. Extra components may be required to meet common mode voltage restrictions of the integrator op amp.

For common current control options, refer to Figure 7. This time the load is central to stability issues because it is inside the feedback loop. Load and filter must be specified right up front.

Type I1 mandates the PWM amplifier to have 2 Isense pins (some models have only 1). This topology does not require high voltage capability for the differential amplifier. For supply voltages above 200V, this is probably the best choice.

Type I2 is required for PWM amplifiers with only one sense pin. This type should also be considered if the filter contains a matching network (type I1 assumes matching network current is delivered to the load). Note a MAJOR change for the diff amp from type I1:

Differential voltage is still usually a volt or less, but Common Mode Voltage (we need to reject this) is up to supply voltage!

This means CMRR is VERY important and buying a packaged instrumentation amplifier is almost always superior to making one. Remember that the basic four-resistor differential amplifier exhibits a common mode rejection error voltage of common mode voltage times the ratio mismatch between the two resistors on the plus input and the two on the minus input. To achieve 80dB CMRR (even with a prefect op amp), resistor mismatch between the plus and minus sides needs to be limited to .01%!

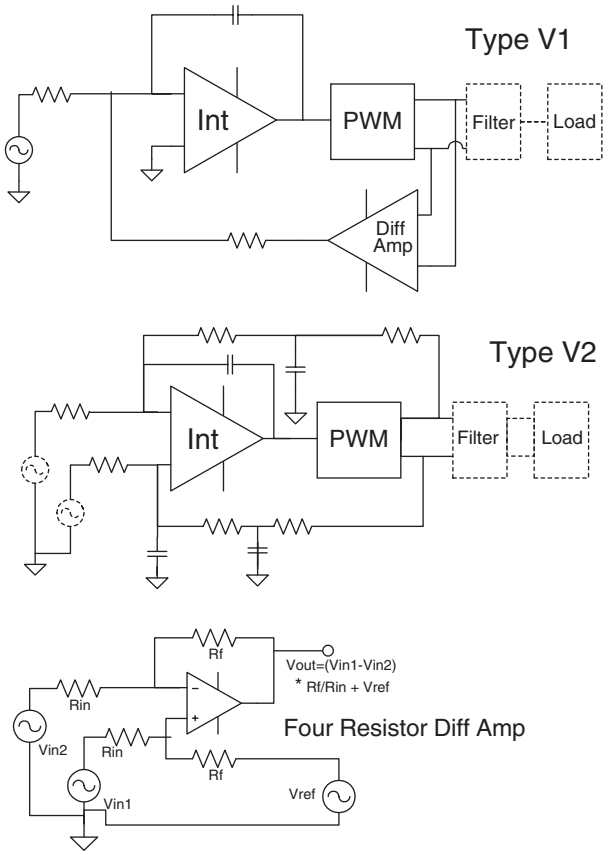


FIGURE 6. BASIC VOLTAGE CONTROL TOPOLOGIES

6.0 TOOLS FOR DESIGN

PowerDesign.exe is a self-extracting spreadsheet for Excel 97 or later. The PWM Stability sheet automates much of this application note, plus includes diagrams and macros for fast

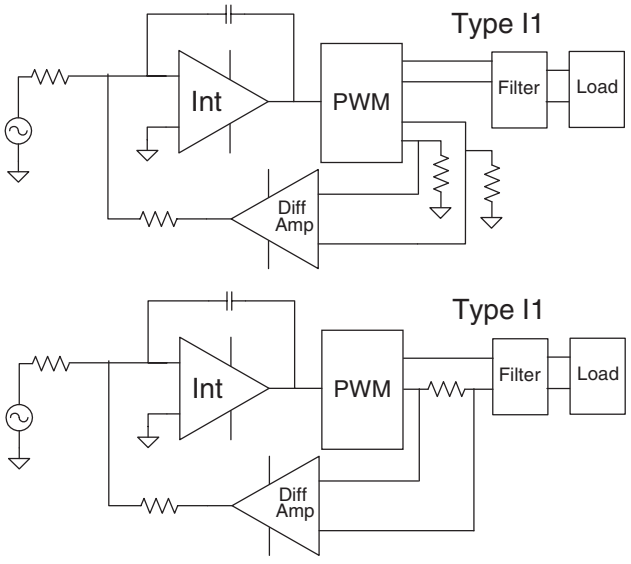


FIGURE 7. BASIC CURRENT CONTROL TOPOLOGIES

execution of common tasks. The liberal use of comments (place cursor in cells with the red triangles) helps the user with both spreadsheet use and with hints and facts on PWM operation. It is the fastest of all the design tools. Its limitations include dedicated topologies, no square wave test, as well as minimal data on maximum bandwidth.

Spice state average models are available for both Berkeley based and Pspice based simulators. With no PWM switching, these models run many times faster than the pulse by pulse models and they can run an AC sweep, making the optimizing of feedback loops very quick once a schematic has been captured. With a Spice platform, topologies are wide open.

Spice macro models are the closest to the hardware of all the tools. Pulse by pulse switching will show some distortion elements the faster tools cannot. They may also show you some capacitors are working harder than you ever imagined, but these additional capabilities may boost simulation time more than two orders of magnitude. Also, these models are not capable of an AC sweep.

So, all three of these software tools agree to your design. This does NOT mean the design is done. There are some things to check which should only be trusted to bench work with real hardware. Significant problems may still exist relating to a mix of high current, high voltage and high frequency all at the same time. When using the fastest PWM amplifiers, one inch of wire in the wrong location can destroy performance. Most readily available op amp models do a poor job of predicting real errors when the input is overloaded with high frequency garbage. While a pulse by pulse model, along with modeling EVERY parasitic would be impressive (and maybe even correct), who has the time and ability to figure size and location of each one?

Before going to the bench, here are a couple of cautions:

1. Even though years of op amp experience may have taught you to start with a reduced load, this can be dangerous with PWM circuits. A reduced load means the filter you designed is improperly terminated, and may produce output voltages far in excess of the supply voltage.
2. Starting with a reduced power supply is fine, as long as you realize bandwidth will increase and phase margin will decrease when the higher design value is applied.

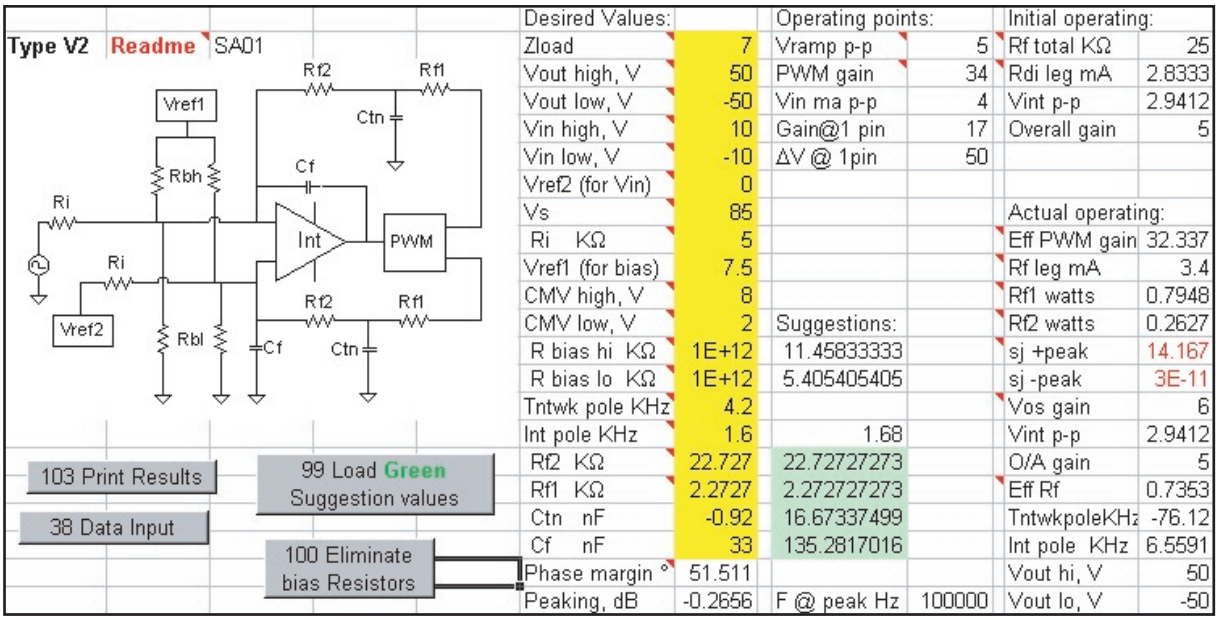
7.0 SIMPLE R-C VOLTAGE CONTROL

EXAMPLE 1

This first example adds to Example 1 from APPLICATIONS NOTE 32, PWM LOW PASS FILTERING. The design critera:

SA01 operating on a 70 to 85V supply
$V_{RAMPp-p}$ = 5V
CMV limits = 2V and 8V
Reference output = 7.5V
Op amp Vos = 10mV
Switching frequency = 42KHz
Output = up to ±50V, from 10Hz to 2KHz
Input signal = ±10V

As the drive system has ±10V available, type V2 topology will be used to yield a simple, low part count circuit. Figure 8 shows the PowerDesign screen after entering SA01, selecting the topology, and the initial data entry. Use command button 100 to eliminate bias resistors and then enter known data in the column of yellow input cells. The first pass selection for R_{IN} was 5KΩ, yielding a ±2mA loading of the drive signal. Suggestions for pole frequencies were used and the Load Green Suggestion Values button was clicked.



Desired Values:		Operating points:		Initial operating:	
Zload	7	Vramp p-p	5	Rf total KΩ	25
Vout high, V	50	PWM gain	34	Rdi leg mA	2.8333
Vout low, V	-50	Vin ma p-p	4	Vint p-p	2.9412
Vin high, V	10	Gain@1 pin	17	Overall gain	5
Vin low, V	-10	ΔV @ 1pin	50		
Vref2 (for Vin)	0				
Vs	85			Actual operating:	
Ri KΩ	5			Eff PWM gain	32.337
Vref1 (for bias)	7.5			Rf leg mA	3.4
CMV high, V	8			Rf1 watts	0.7948
CMV low, V	2	Suggestions:		Rf2 watts	0.2627
R bias hi KΩ	1E+12	11.45833333		sj +peak	14.167
R bias lo KΩ	1E+12	5.405405405		sj -peak	3E-11
Tntwk pole KHz	4.2			Vos gain	6
Int pole KHz	1.6	1.68		Vint p-p	2.9412
Rf2 KΩ	22.727	22.72727273		O/A gain	5
Rf1 KΩ	2.2727	2.272727273		Eff Rf	0.7353
Ctn nF	-0.92	16.67337499		TntwkpoleKHz	-76.12
Cf nF	33	135.2817016		Int pole KHz	6.5591
Phase margin °	51.511			Vout hi, V	50
Peaking, dB	-0.2656	F @ peak Hz	100000	Vout lo, V	-50

FIGURE 8. INITIAL DATA ENTRY AND PRELIMINARY CHECKS FOR TYPE V2 CIRCUITS

The two feedback resistor suggestions are a convenient split totaling the value (appears in the upper right corner) required to meet overall gain specified, with the 5KΩ input resistor. The 1/11 split means the loading effects of the larger resistor on the pole, created by the smaller resistor and the capacitor, will be at a minimum. After a standard value is entered for R_{F2}, the suggestion for R_{F1} is recalculated as the ideal total minus R_{F2}. The feedback pole frequency reported here, is calculated as though the larger resistor did not exist. It is perfectly acceptable to use both resistors equal to half the R_F total value given. The 1/ßeta plot, the peaking, and phase margin will still be correct. Now is the time for two preliminary checks.

First check the will be power ratings for the two feedback resistors. The resistor connected directly to the PWM outputs must be checked for AC power. With the associated pole fre-

quency being substantially less than the F_{SW}, the impedance of the capacitor will be much less than that of the resistor. Assume a square wave of ±Vs/2 is applied to approximate the reported power for this resistor. The second resistor power rating is reported as a DC function, assuming the PWM output pin is being held at Vs. Notice that with a 5KΩ input resistor, there is nearly 3/4W in the smaller resistor. It was decided to change R_{IN} = 15KΩ, which will allow a 1/2W resistor to handle the job with some margin. New values for R_{F2} and R_{F1} will be 68.1KΩ and 6.9KΩ. The second check to be made is to see if the suggested capacitor values are in a convenient range. Increasing R_{IN} will decrease capacitor values.

After entering the new input resistor value and loading suggestions, we need to turn our attention to biasing and CMV. Refer to Figure 9A for the most important new numbers. With no bias resistors, we have problems on both ends of the CMV window. Lets attack the lower side by entering roughly the suggested value, 33K for the high side bias resistor. This suggestion is a DC calculation of the resistor required to pull the combination of R_F (assuming V_{OUT} = 0) and R_{IN} up to the lower CMV limit when connected to VREF. In Figure 9B, the lower CMV limit has been met but the upper is still too high. The second suggestion appears and is 33KΩ *ΔCMV / Δsj peak. To rephrase, the 19.1KΩ is the 33KΩ lowered by the amount that the $V_{SJ\ p\text{-}p}$ is still too high. When the 19.1KΩ is entered as in section C, the reported VSJ peaks are both too high. The 17KΩ suggestion for the lower bias resistor is a DC calculation of the resistor needed to pull down the combination of R_F (assumes $V_{OUT} = V_S$), $R_{BIAS\ HI}$ and R_{IN}, to the upper CMV limit. In section D, the 16.9KΩ has been entered, the summing junction voltages meet the CMV limits, and voltage offset gain is ~14.3. Use this gain to calculate Vos, NOT signal gain.

CMV low, V	2	Suggestions:		Rf2 watts	0.0875
R bias hi K	1E+12	34.375		sj +peak	14.167
R bias lo K	1E+12	16.21621622		sj -peak	9E-11

A

CMV low, V	2	Suggestions:		Rf2 watts	0.0875
R bias hi K	33	34.375	19.2706	sj +peak	12.335
R bias lo K	1E+12	16.73003802		sj -peak	2.0604

B

CMV low, V	2	Suggestions:		Rf2 watts	0.0875
R bias hi K	19.1	34.375	13.3835	sj +peak	11.53
R bias lo K	1E+12	17.12492528		sj -peak	2.9668

C

CMV low, V	2	Suggestions:		Rf2 watts	0.0875
R bias hi K	19.1	34.375	19.3668	sj +peak	7.9675
R bias lo K	16.9	-1861.9363		sj -peak	2.0502
Tntwk pole KHz	4			Vos gain	14.365

D

FIGURE 9. CHANGES DUE TO THE 15KΩ INPUT RESISTOR

The process varies with application, but basics of selecting bias resistors are:

The high bias resistor has the most affect on V_{SJ} -peak.

The low bias resistor has the most affect on V_{SJ} +peak.

Selection assumes PWM outputs reach 0 & V_S (a safety margin).

Selection is an iterative process.

A near perfect selection results in:

High bias actual = second suggestion (19KΩ here).

Low bias suggestion = a large number of either polarity.

Summing junction voltages close to specified limits.

Less than perfect selection results in increased Vos gain.

1/ßeta plot may change quite a bit at low frequencies.

With feedback resistor power levels and DC biasing out of the way, we can turn to stability. There are only two decisions to be made here, the T-network pole and the integrator pole frequencies. The T-network pole placement relative to F_{SW} determines what fraction of the square wave output is fed back to the integrator. A good place to be is 1/10 of F_{SW}, where coincidentally, the fraction is about 1/10. The second decision is picking a fraction of the T-network pole to assign to the integrator pole. The rule of thumb is 0.4. Smaller fractions tend to yield more stable circuits at the expense of system bandwidth. Capacitor values for the frequencies entered are suggested automatically. Initial results of entering 4.2KHz for the T-network and 2KHz for the integrator (this is our system requirement), are shown in Figure 10.

Ctn nF	5.4919	5.491888996	
Cf nF	36.075	36.07512043	
Phase margin	39.438		
Peaking, dB	2.0357	F @ peak Hz	3651.74

FIGURE 10. INITIAL STABILITY CHECK ON THE SHAKER TABLE DRIVE.

The job now is to find standard values, which will maintain or improve phase margin without reducing the integrator pole below 2KHz. Figure 11 shows our choices.

Ctn nF	4.7	5.491888996	
Cf nF	33	36.07512043	
Phase margin	39.935		
Peaking, dB	1.9317	F @ peak Hz	4216.97

FIGURE 11. FITTING THE CIRCUIT TO STANDARD VALUE COMPONENTS

Additional steps used to verify this design are shown in Figures 12-14 (this and next page) . The first two utilize the state average spice models with each analysis requiring only a few seconds simulation time. The AC sweep indicates the circuit is only 0.85dB down at 2KHz. The square wave test agrees with Power Design in saying we have adequate phase margin. This model could also show us that supply current is substantially less than the ~7A delivered to the load. Next is the pulse by pulse simulation which required 4 minutes simulation time on a 750MHz PC. This model could also provide vast quantities of switching waveform data. Last is the hardware square wave test. This is the only test verifying that the op amp is not getting into trouble with high frequency common mode voltage.

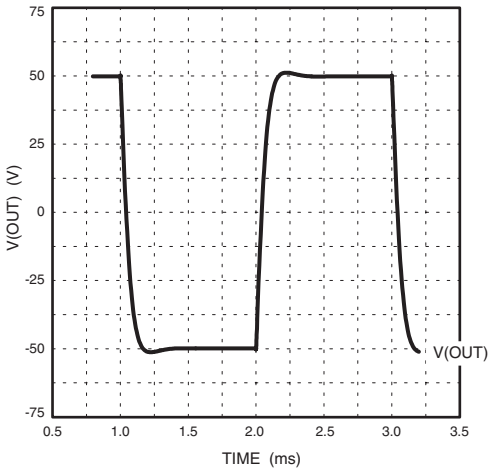


FIGURE 12. STAGE AVERAGE SPICE MODEL SQUARE WAVE TEST

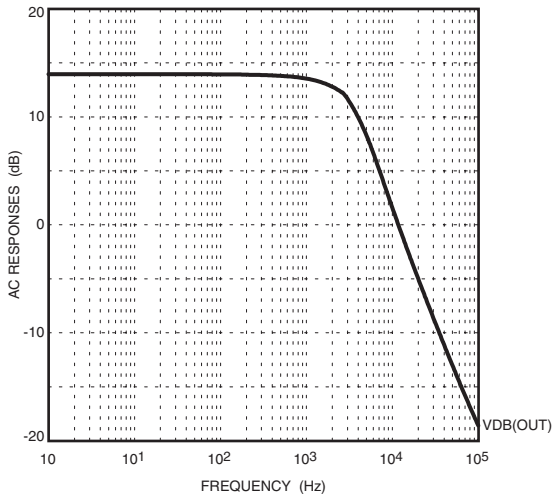


FIGURE 13. STATE AVERAGE SPICE MODEL AC SWEEP TEST

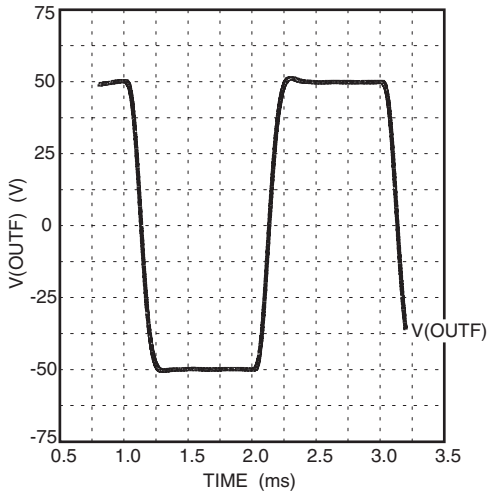


FIGURE 14. PULSE BY PULSE SPICE MODEL SQUARE WAVE TEST

EXAMPLE 2

Here's the given data for this example:

MSA260, half bridge mode operation

Vcc = 15V, Vs ranges from 156V to 178V

Switching frequency = 20KHz

Output = 10.2 to 53V, basically a DC amplifier

Load resistance = 3.7Ω at low output, 5.2Ω at high output

Makes use of the onboard error amplifier and voltage reference

This example is extracted from Power Design, PWM Examples sheet where details of product selection, filter and inductor design and heatsink selection are also covered. The topology of Figure 15 will be used in this example. While the filter and load are part of the system, the first order stability analysis is not affected by their values and you will enter only load resistance which is used to approximate internal voltage loss.

Type V3 is limited to half bridge operation and is easiest to understand with non-inverting PWM operation from the PWM input to the output (the percentage of time the output is high increases as the analog input increases). Alternately, the integrator can be used upside down (ground the -input and connect the passive component to the +input) with an inverting PWM function. Some applications may require Rbh, some Rbl, and some do not require either bias resistor.

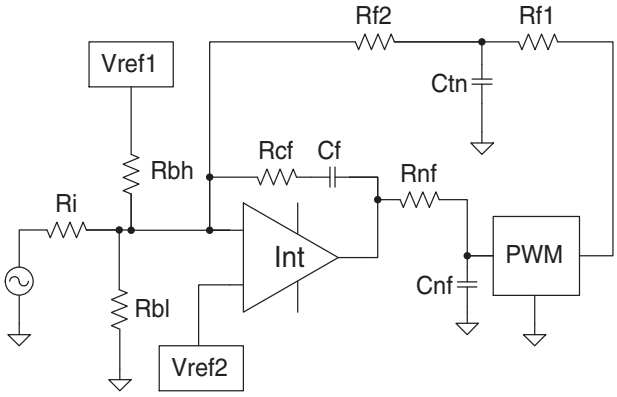


FIGURE 15. The simplest of all closed loop PWM systems is Type V3.

Initial data entry into Power Design is shown in Figure 16. Here are some entries that may not be obvious:

1. Zload is the mid range of the load impedance.
2. Vref2 must be within the common mode range of the integrator (0 to 4V for the MSA260), usually positive, and a lower amplitude than Vref1.
3. Setting Ri to 5K just seemed a reasonable starting point.
4. The MSA260 provides a 5V reference.
5. The high bias resistor was left open because the suggested value was negative.
6. The suggested value for the low bias resistor was entered.
7. Pole frequencies were more conservative than the suggestions in the comments because we have virtually no bandwidth concerns.
8. The command button to Load Green Suggestions was used.
9. Rcf is normally only used in servo loops.
10. Rnf and Cnf put a noise filter pole at 15.9KHz, a good design practice.

Desired Values:		Operating points:		Initial operating:	
Zload	4.5	PWM gain	89	Rf total KW	21.4
Vout high, V	53	Vin ma p-p	2	Rf leg mA	6.7424
Vout low, V	10.2	Gain@1 pin	89	Vint p-p	0.4809
Vin high, V	0	DV @ 1pin	42.8	Overall gain	4.28
Vin low, V	10			I FDBK High	2.3598
Vref2 (for Vin)	2.5	Rcf KW	0	I In High	-0.5
Vs	178	Rnf KW	1	Delta Isj	1.8598
Ri KW	5	Cnf nF	10	Actual operating:	
Vref1 (for bias)	5			Eff PWM gain	85.486
				Rf leg mA	8.3178
		Suggestions:		Rf1 watts	4.0715
R bias hi KW	1E+12	-1.34422111		Rf2 watts	1.346
R bias lo KW	1.344	1.344221106		Vos gain	21.203
Tntwk pole KHz	1			Vint p-p	0.5007
Int pole KHz	0.3	0.4		O/A gain	4.28
Rf2 KW	19.455	19.45454545		Eff Rf	0.2503
Rf1 KW	1.9455	1.945454545		Rcf zero KHz	#DIV/0!
Ctn nF	81.809	81.80861561		NoisepoleKHz	15.915
Cf nF	2119.2	2119.229685		TntwkpoleKHz	1
Phase margin °	41.941			Int pole KHz	0.3
Peaking, dB	1.5211	F @ peak Hz	749.894	Vout hi, V	53.007
				Vout lo, V	10.207

FIGURE 16. Is this a complete design?

While the values in Figure 16 would produce a working circuit, please check the 4W rating for Rf1 on the right and the large Cf on the left. All component values in the lower half for Figure 16 are scaled to the specified value of Ri. Figure 17 shows all the rescaled values and operating parameters when Rin is increased to 20K.

Desired Values:		Operating points:		Initial operating:	
Zload	4.5	PWM gain	89	Rf total KW	85.6
Vout high, V	53	Vin ma p-p	0.5	Rf leg mA	1.6856
Vout low, V	10.2	Gain@1 pin	89	Vint p-p	0.4809
Vin high, V	0	DV @ 1pin	42.8	Overall gain	4.28
Vin low, V	10			I FDBK High	0.59
Vref2 (for Vin)	2.5	Rcf KW	0	I In High	-0.125
Vs	178	Rnf KW	1	Delta Isj	0.465
Ri KW	20	Cnf nF	10	Actual operating:	
Vref1 (for bias)	5			Eff PWM gain	85.486
				Rf leg mA	2.0777
		Suggestions:		Rf1 watts	0.893
R bias hi KW	1E+12	-5.37688442		Rf2 watts	0.3315
R bias lo KW	5.36	5.376884422		Vos gain	21.267
Tntwk pole KHz	1			Vint p-p	0.5011
Int pole KHz	0.3	0.4		O/A gain	4.2835
Rf2 KW	76.8	77.81818182		Eff Rf	1.0022
Rf1 KW	8.87	8.8		Rcf zero KHz	#DIV/0!
Ctn nF	18	17.9430601		NoisepoleKHz	15.915
Cf nF	470	529.3745216		TntwkpoleKHz	0.9968
Phase margin °	41.242			Int pole KHz	0.3379
Peaking, dB	1.6625	F @ peak Hz	805.842	Vout hi, V	53.167
				Vout lo, V	10.332

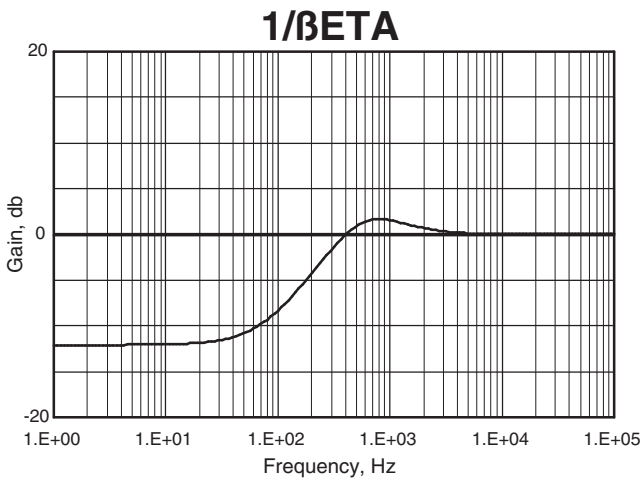


FIGURE 17. The final design values and operating parameters.

Power Design makes it easy to check component tolerances for both DC and dynamic performance, as shown in Figure 18. The top group indicates our choice of standard values places the output voltages within 167mV of nominal. In the second group, reference voltage divider accuracy is altered 1% (integrator voltage offset is also in series with the reference voltage) to find maximum error to be 0.7V. The next group pegs error at 0.45V for a 1% change in Ri. The next two groups show similar errors for variations of the bias resistor and the larger feedback resistor. As phase margin decreases when the two pole frequencies get closer together, the last group shows that the worst 10% changes in capacitance have very little effect.

8.0 VOLTAGE CONTROL WITH A DIFFERENCE AMPLIFIER

Refer to Figure 19 for the general type V1 topology while various options are covered. The schematic shown here may contain more parts than you actually need because there are three options to cover.

Option 1: As drawn, this is a full-bridge PWM with the diff Amp. For half-bridge applications, the diff amp becomes a simple inverting op amp circuit with Vref1 tied to the non-inverting input.

Option 2: Op amp supplies may be single or dual. If dual supplies are used (usually only done when already available in the system), Vref1 becomes ground. This makes for a "clean" circuit where voltages out of the diff amp

Vref2 (for Vin)	2.5		
Ri KW	20	Vout hi, V	53.1668
R bias lo KW	5.36	Vout lo, V	10.3318
Rf2 KW	76.8		
Vref2 (for Vin)	2.525		
Ri KW	20	Vout hi, V	53.6984
R bias lo KW	5.36	Vout lo, V	10.8634
Rf2 KW	76.8		
Vref2 (for Vin)	2.5		
Ri KW	20.2	Vout hi, V	53.0607
R bias lo KW	5.36	Vout lo, V	10.6499
Rf2 KW	76.8		
Vref2 (for Vin)	2.5		
Ri KW	20	Vout hi, V	52.7682
R bias lo KW	5.414	Vout lo, V	9.93323
Rf2 KW	76.8		
Vref2 (for Vin)	2.5		
Ri KW	20	Vout hi, V	53.6222
R bias lo KW	5.36	Vout lo, V	10.4022
Rf2 KW	77.57		

Ctn nF	18	Ctn nF	18.18
Cf nF	470	Cf nF	423
Phase margin °	41.242	Phase margin °	40.488
Peaking, dB	1.6625	Peaking, dB	1.8171

FIGURE 18. Checking component tolerances.

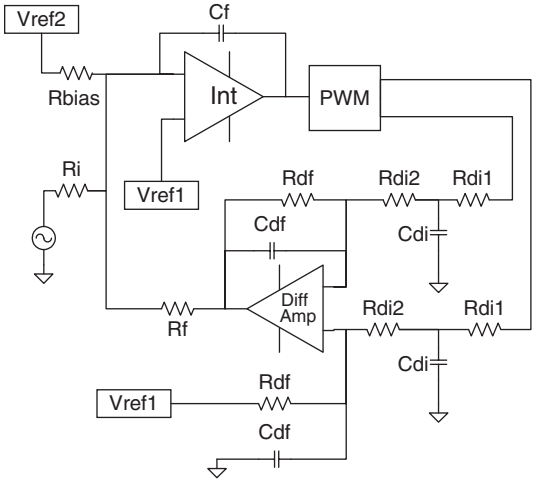


FIGURE 19. "ONE SIZE FITS ALL" VERSIONS OF CONTROLLING VOLTAGE WITH A DIFF AMP.

and into the integrator are proportional to and not level shifted from the actual output voltage. If a single supply is used, Vref1 as shown will allow the diff amp output to swing negative with respect to Vref1 (required to close the feedback loop).

Option 3: If the input signal needs shifting, Vref2 can be assigned a value higher than Vref1, or below ground, so that Rbias will provide the proper shift. Consider:

A. The half- bridge output never goes negative, but the input signal is bipolar with respect to Vref1. This would be the case with bipolar input signals (single or dual supplies, Vref1=ground or above) or when input signals range from 0 to a positive level and the op amps are on a single supply (Vref1 is above ground). If Vref2 is more positive than

Vref1, Rbias is capable of providing the shift. See Figure 20 for the half-bridge version of this circuit

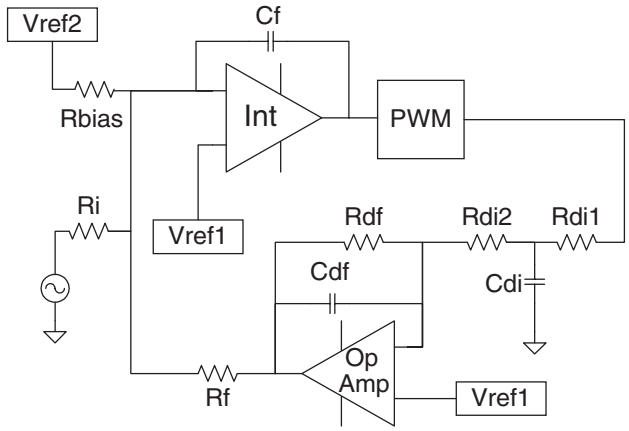


FIGURE 20. THE HALF-BRIDGE VERSION IS SIMPLER THAN THE FULL BRIDGE

B. The full-bridge output swing is bipolar, but the input signal range is not spread equally above and below Vref1.

I. This could happen with bipolar input signals and single supply operation (Vref1 is above ground). If Vref2 is more positive than Vref1, Rbias is capable of providing the shift.

II. This could also occur when the input signal ranges from 0 to a positive value and the op amps are running on dual supplies (Vref1 = ground). If Vref2 is below ground, Rbias is capable of providing the shift.

C. With this general technique, even a voltage derived from a 4/20mA loop could be shifted to program a symmetric bipolar output or a unipolar output including zero. The idea is to compute input current for an input signal voltage where no current flows through R_F, and make current provided by RBIAS equal and opposite. For full bridges, this input voltage corresponds to 0V output. For half bridges, this input voltage corresponds to an output voltage equal to Vref1.

This circuit in Figure 20 could be implemented using dual supplies for the op amps, but additional circuitry must be added to prevent integrator output swing below ground. Such an event would be in violation of the Absolute Maximum Input Voltage range of the PWM amplifier. Even if this caused no damage, a swing below the lower ramp peak does not result in any further voltage change at the output. It merely puts a big non-linearity in the system.

9.0 WHAT'S DIFFERENT ABOUT CURRENT CONTROL?

It's already been mentioned that the filter and the load are inside the loop for a current control application, but here are a few more handy-to-know details. In applications where the load does most of the filtering, such as servos, the "filter" is often far from that described in Application Note 32. Instead, the filter only knocks off the sharp edges of the raw output, and the load mainly does the job of demodulating the signal from the carrier. The tricky part lies in the load that usually contains moving parts and the mechanical factors need to be equated to electrical parameters for a complete analysis of the system.

Even when there is a filter in the more normal sense, it often diverges from textbook design when it comes to the matching network. The textbook filter includes this network if the load has any reactive elements because a flat pass band requires the load to appear resistive to the filter. One way to think of the network/load relationship is that any frequency change induced decrease of load current is accompanied by an equal increase of network current making the total impedance appear constant. A second way to view this situation is the amplifier output current is never equal to load current. Because monitoring amplifier output current is the easiest way to implement current control, the network impedance is often larger than ideal, the filter is not ideally terminated, and the output voltage at the load peaks near F_C. It would be a good idea to keep this voltage mode peaking down to no more than 10dB.

10.0 CURRENT CONTROL USING THE ISENSE PINS

EXAMPLE 3

This application provides current drive for a coil. Bandwidth of the circuit needs to be DC to 2.5KHz. Here's the rest of the given data for this example:

SA12 full bridge amplifier
- Vcc = 15V
- $V_{RAMPp\text{-}p}$ = 4V
- Switching frequency = 200KHz
- Input signal = 2.5 to 7.5V

Load impedance = 0.3mH, 9Ω
Load current = ±10.2Apk
System does not have a negative supply

For a quick way to find required voltage drive, use the Power Design, Power sheet. For this load to reach the required current at maximum frequency, it will need 103.5V peak swing. The answer explaining why a PWM was selected is also on this sheet; a perfect linear solution for this drive will need to dissipate 312W and most real op amps weigh in at 350 or more watts. The next stop will be the PWM Filters sheet. F_C was set at 20KHz, second order component values were rounded off, except the resistive component of the matching network was doubled. In the PWM Power sheet, signal drive was set to voltage control for a peaking test. See Figure 21 for the results.

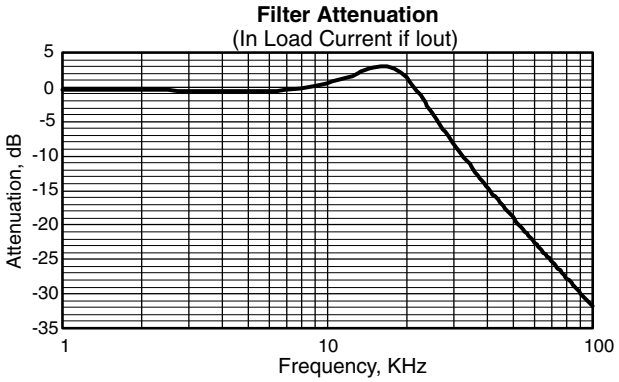


FIGURE 21. TESTING THE FILTER/LOAD FOR PEAKING IN THE VOLTAGE MODE

With all the preliminaries out of the way, (including selection of a 120V for the main supply), the next stop is the PWM Stability sheet. In the top left corner of this sheet, SA12 in entered and the Type I1 configuration is selected. Figure 22 (next page) shows the area where the filter, matching network and load can be entered manually or extracted from our previous work. For first pass analysis, leave the inductance of the load equal to zero. If you started with the PWM Filters sheet, this inductance will be the lower right cell.

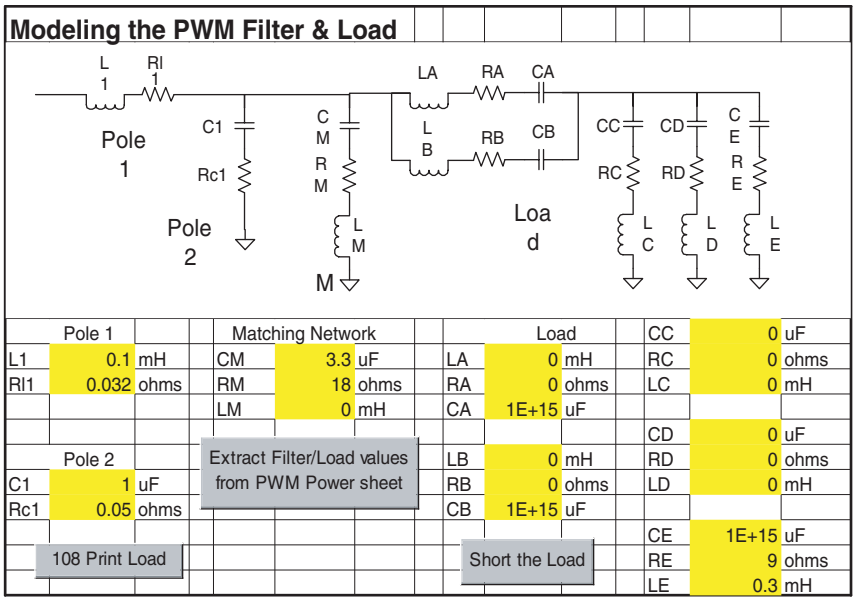


FIGURE 22. SETTING UP THE FILTER, MATCHING NETWORK AND LOAD FOR STABILITY

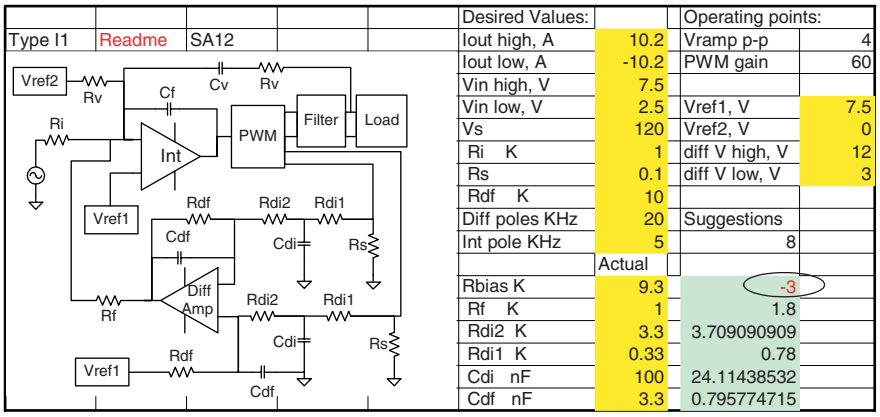


FIGURE 23. CIRCUIT SET UP FOR CURRENT CONTROL USING THE PWM ISENSE PINS.

Figure 23 illustrates more circuit set up. Given data is entered and the first circuit choice is a value for the input resistor. A range between 1 and 10KΩ usually avoids both excessive loading of the signal source and high impedance nodes that tend to either kill bandwidth, pick up noise or oscillate.

There are two logical choices for sense resistor values; the one that will develop the voltage required for activation of the SA12 current limit function (100mV) and the value to develop about 1V (a safe level which will not affect the switching action of the lower MOSFETs). From both the accuracy and bandwidth points of view, a higher voltage is better. Choices of value for R_{DF} cover a wide range and this choice will scale values for the input resistors and the roll off capacitors. Very low values can demand capacitors larger than practical and very high values can bring on problems with op amp offset current errors (bipolar input types) or can allow circuit parasitics too much influence on pole frequencies. A good goal would be make sure all capacitors used are at least 100pF. The recommendation of $F_{SW}/10$ was used for the diff amp pole placement and a slightly more conservative entry for the integrator pole was made. The diff amp will be LF353, running on the 15V required for the SA12 Vcc supply and the appropriate swing limitations were entered for Diff V high and low. Vref1 was set at half the op amp supply to allow the diff amp to swing symmetrically.

At this point, Vref2, the rest of the Actuals and the suggestions are all left over from the last circuit development. Even so, we have useful information in the suggestion for Rbias; it is negative and printed in red. This means the bias reference, Vref2 is the wrong polarity with respect to Vref1. The spreadsheet has followed the guidelines above for level shifting: find Vin (5V) for zero current out (no current in R_F); find input current at Vin=5V (Δ2.5V/1KΩ), and calculated the resistor needed to provide an equal but opposite current from Vref2 (Δ7.5V/-2.5mA). Entering an easily obtained 10V for Vref2, results in a new Rbias suggestion of 1KΩ.

The suggestion for R_F will place diff amp swing exactly at the limits specified above. Entering an Actual value higher than the suggestion will demand greater diff amp swing. The suggestion for Rdi2 will be 10/11 of the total required to meet diff gain for the overall transfer function. Entering a close standard value will recalculate the suggestion for Rdi1 making up the remainder of the total input resistance. This decade relationship between the two input resistors is not mandatory, but is clean in that Rdi2 will have very little effect on the pole of Rdi1 and Cdi. If you are happy with the high and low output values in the lower right of Figure 24, this completes setup of gain and biasing. If this is not the case, check for standard values of better tolerance resistors (0.1% instead of 1% or 5%), or consider adding adjustment networks for offset and gain. While thinking of DC error budgets, move up this column to find output current errors corresponding to the voltage offset of the integrator and diff amp op amps.

	Actual				
Rbias K	1	1		Int Vos, A/V	10.419
Rf K	1.8	1.8		Diff Vos, A/V	12.265
Rdi2 K	2.05	2.060606061		Iout p-p	20.385
Rdi1 K	0.215	0.216666667		O/A Xfer, A/V	4.077
Cdi nF	33	37.01277746		Eff Rf @.01Hz	0.6552
Cdf nF	1	0.795774715		Diff pole i KHz	22.432
Cf nF	47	48.58403031		Diff pole f KHz	15.915
Cv nF	999	1.28652E-05		Int pole KHz	5.1685
Rv K	1E+07	64.86209964		RvCvpoleKHz	2E-08
Phase margin °	18.379	7.826086957		Beta @.01Hz	0.5973
Peaking, dB	7.7364	F @ peak Hz	8659.64	Iout high, A	10.193
				Iout low, A	-10.19

FIGURE 24. CHECK THE DC ERROR BUDGET AND START STABILIZING THE CIRCUIT

Stabilizing the circuit will be an iterative process. The first step is to set up the circuit for about 10dB peaking with NO inductive load. In Figure 24, note that Actuals have been entered for the first three capacitors using standard values similar to the suggestions. It is important that Cv and Rv have large values for this first phase. Note that our entries result in a little under 8dB peaking at about 8.7KHz. Peaking below 10dB will not endanger the final stability solution but will lower bandwidth. Higher values of peaking will make the

final stability solution very elusive. Increasing the integrator capacitor, Cf will decrease peaking. Increasing the diff amp capacitors will increase peaking. Another way to put all this is that peaking will decrease as the ratio between integrator and diff amp pole frequencies widens. Beware: decreasing diff amp capacitors allows more high frequency energy to reach the op amp. When satisfied with this step, use the command button to Define the Filter/Load, and reinsert the correct value for load inductance. If your specific application has no load inductance, adjust Cf for a phase margin of at least 30° (more is better, if you can afford the bandwidth), and you are finished.

Figure 25 shows the results of re-entering the load inductance value; peaking is too high, phase margin is too low. Start with the higher suggestion given for Rv and zero in on a value range yielding 1 to 4dB peaking, and then enter the suggested value for Cv. The upper suggestion is designed to limit 1/ßeta to 10dB above the value calculated at 0.01Hz. The lower suggestion is designed to limit to 3dB. Figure 25 shows our final component selection and the 1/ßeta plot results. The circled area in both plots is the result of the voltage mode peaking in the filter/load because the matching network impedance was doubled from design value. Figure 21 shows this peaking in the load. See Figure 26 for square wave test results with both state average and macro models.

11.0 CURRENT CONTROL USING A SERIES LOAD SENSE

EXAMPLE 4

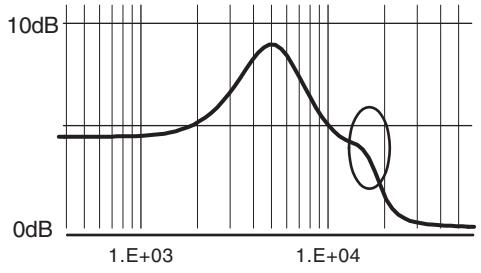
This application provides current drive for a motor. Bandwidth of the circuit needs to be DC to 100Hz. This circuit is part of a DSP based system controlling elevation and azimuth of an antenna. Here's the rest of the given data for this example:

SA01 operating on 48VDC.
$V_{RAMPp-p}$ = 5V
Switching frequency = 42KHz
Input signal = ±4.2V
Load impedance = 0.3mH, 1.5Ω
Load current = ±16.7Apk
Diff amp is INA117 running on ±15V
Op amp is LT1013 running on ±15V

To avoid significant phase shift in the filter, its design approach was very different from the normal design for a voltage output circuit. The objective is to knock off the square edges of the PWM waveform and reduce the peak to peak amplitude to roughly a third of the 48V supply. At $F_{C,}$ motor impedance will be very high, leaving the matching network as the prime termination of the filter, and the prime factor in determination of ripple current. It was decided that

Cv nF	999	2.2878E-05	
Rv K	1E+07	64.86209964	
Phase margin °	28.966	7.826086957	
Peaking, dB	4.4834	F @ peak Hz	4869.68

A



Cv nF	3.3	3.614914215	
Rv K	51	64.8622161	
Phase margin °	40.046	7.826086957	
Peaking, dB	1.9085	F @ peak Hz	6042.96

B

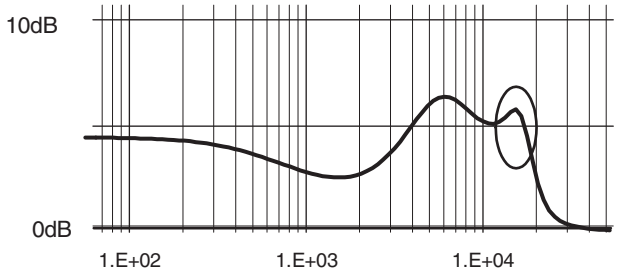


FIGURE 25. FINAL STEPS OF COMPONENT SELECTION FOR TYPE I1 CIRCUITS

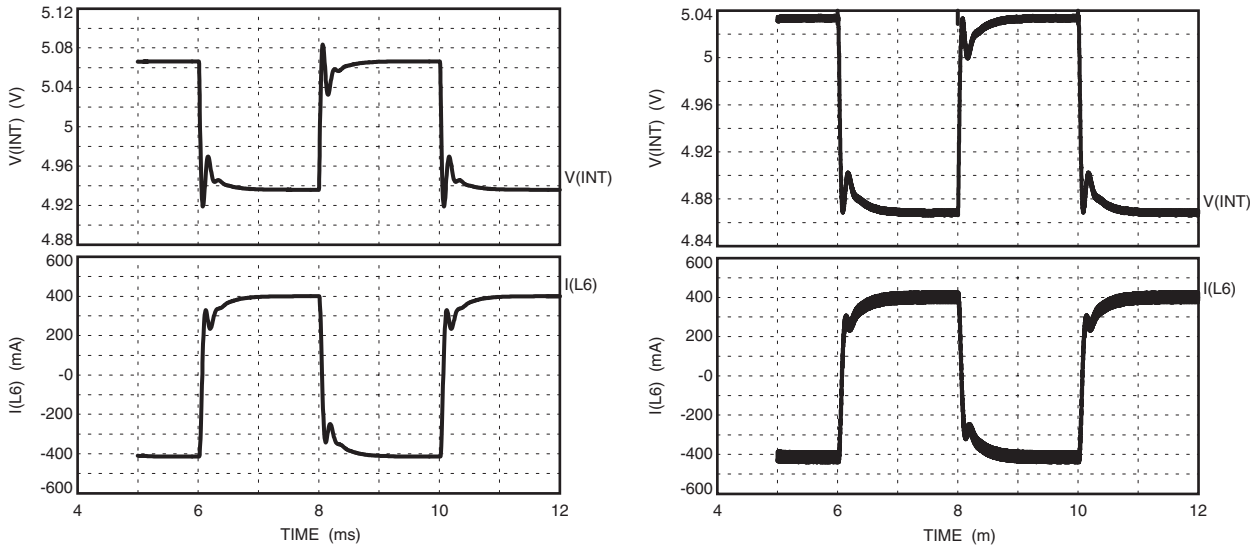


FIGURE 26. SQUARE WAVE TESTING EXAMPLE 3

1.5Ap-p ripple current would be acceptable. With ripple voltage being roughly 16Vp-p, 10Ω would be a reasonable impedance for the matching network. Examination of ideal attenuation graphs indicates a second order filter set at 1/2 F_{SW} should yield a -10dB response (about a third). Loading 21KHz, 10Ω and 300µH into the PWM Filters sheet yielded (adjusted to standard components) 47µH and 1µF to ground for each output, plus a matching network of 3.3µF and 10Ω. A check with the PWM Power sheet (voltage drive mode and the real 1.5Ω motor resistance) reveals -10.5dB at 42KHz and no peaking.

Refer to Figure 27 for data input in the PWM Stability sheet. Parasitic values for pole 1 and 2 elements were defaults calculated. Note that for the first pass stability calculations, the load inductance was set to zero. At the second pass this will be re-entered as 0.3mH. All the given data is entered below this and some circuit choices will be made. The input resistor choice was arbitrary. The sense resistor value was a trade off between voltage loss at high currents and accuracy errors caused by the voltage offset of the INA117. The INA117 data sheet also indicates 1KΩ in series with its inputs will not seriously degrade performance, and this value will allow reasonable filter capacitor values

Rbias K	10	1E+12									
Rf K	3.97	3.966274789									
Cdi nF	33	39.78873577									
Cfilt nF	100										
Copf nF	3.3	3.978873577									
Cf nF	27	25.01684876									
Cv nF	999	0.000673238									
Rv K	999999	125.9623149									
Phase margin ∞	19.101	14.16276477									
Peaking, dB	7.4752	F @ peak Hz	1654.8								

LE	0.3	mH									
Don't forget me!											
Cv nF	22	19.10162495									
Rv K	47	125.9658199									
Phase margin ∞	32.422	14.16276477									
Peaking, dB	3.6139	F @ peak Hz	1240.9								

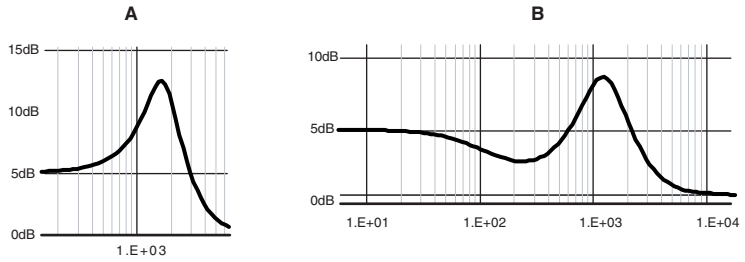


FIGURE 28. STABILIZING THE TYPE I2 CURRENT OUTPUT CIRCUIT

Pole 1			Matching Network			Load			CC	0	uF
L1	0.094	mH	CM	3.3	uF	LA	0	mH	RC	0	ohms
Rl1	0.0482	ohms	RM	10	ohms	RA	0	ohms	LC	0	mH
			LM	0	mH	CA	1E+15	uF			
									CD	0	uF
Pole 2									RD	0	ohms
C1	0.5	uF				LB	0	mH	LD	0	mH
Rc1	0.1	ohms				RB	0	ohms			
						CB	1E+15	uF	CE	1E+15	uF
									RE	1.5	ohms
									LE	0	mH

Type I2	Read me	SA01	Desired Values:		Operating points:	
			Iout high, A	16.7	Vramp p-p	5
			Iout low, A	-16.7	PWM gain	19.2
			Vin high, V	4.2	Vref1, V	0
			Vin low, V	-4.2	Vref2, V	0
			Vs	48	Vref3, V	0
			Ri K	10	o/a gain: +/-	-
			Rs	0.01	Ropin K	1
			Diff amp gain	1	Ropf K	10
			Rdi K	1	Rfilt K	10
			Rzin K	400		
			fdbk poles KHz	4	Suggestions	
			Int pole KHz	1.6	1.6	
				Actual		
			Rbias K	1E+12	1E+12	

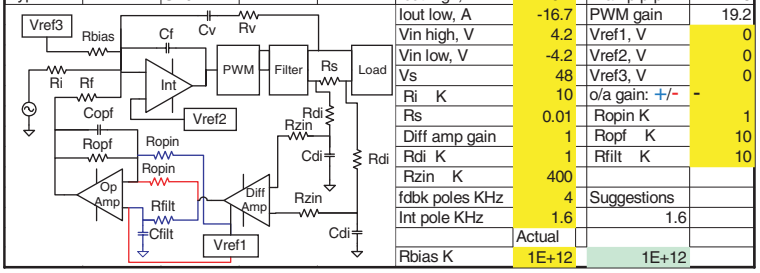


FIGURE 27. SETTING UP EXAMPLE 4 FOR STABILITY ANALYSIS

in the few KHertz range. The 400KΩ input impedance was also extracted from this data sheet. Pole frequency for the feedback poles are set at 1/10 F_{SW} and the suggestion for the integrator pole frequency was used.

As no level shifting was required for this circuit, all references were set to zero. Again, arbitrarily, inverting gain for the op amp was entered. This could be changed to non-inverting as long as the two inputs to the diff amp were also reversed. The 1K/10KΩ gain setting for the op amp seemed convenient. The possibilities for specific component values have great latitude in several areas as long as related components are scaled in a similar fashion. When making specific choices, check effects of amplifier bias currents, voltage offset effects on current output, and keep impedances low enough such that a stray capacitance of 10pF will have negligible effect on the circuit.

The A side of Figure 28 shows suggestions, standard values entered and results for Step 1 where inductance has been removed from the load. Note that a bias resistor of 10KΩ was entered. Rather than biasing, this resistor serves as an auxiliary input for offset adjust and a velocity loop input. As entered, this resistor has no effect on DC output but it does change the feedback factor, and consequently the stability solution. The 7.5dB peaking level is a little on the conservative side. The first choice for Rv in the second step (inductance re-entered) was 39Ω. After running the square wave test with a state average model, it was decided to change Rv to 47KΩ as shown in the B side.

By now, some of you have realized there are significant details missing in the presentation of this circuit. The integrator was set up for ±15V, the SA01 on-board op amp is normally used as the integrator, and it is single supply only and requires a reference voltage to avoid common mode voltage violation. Refer to Figure 29 to see the actual implementation. Here are some reasons for this approach:

1. The INA117 data sheet does not mention single supply operation.
2. Reference voltage for the INA117 needs to be zero impedance (requiring an op amp rather than a simple voltage divider).
3. Voltage offset of the SA01 op amp is 10mV; drift is not specified.
4. Driving an SA01 input pin directly with negative voltage violates Absolute Maximums.

With the INA117 on dual supplies and using ground as the reference voltage, items 1 and 2 above are no problem. By using the SA01 op amp as a level shifter, item 4 above is taken care of. As long as the level shift function has a gain of one, there will be no changes in AC performance. This

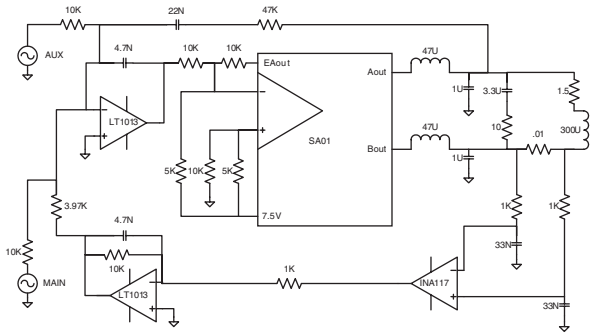


FIGURE 29. SOLVING SEVERAL CIRCUIT LIMITATIONS WITH UNUSUAL TOPOLOGY

also places the offset and drift of the SA01 op amp inside the loop of the actual LT1013 integrator with much better accuracy (item 3).

During circuit development, several variations of the filter and matching network system were evaluated. In addition to the 1/ßeta plot and square wave test, voltages at the input to the diff amp, on the wires leading to the motor and across the motor, were analyzed with an input of 0V. Refer to Figures 30 through 34 for the following points:

1. The only option causing a significant change in the 1/ßeta plot or the square wave test is the use of large filter capacitors and no matching network. The reason for the dip below 0dB at 27KHz is very high voltage mode peaking as shown in Figure 34 (next page). We already knew this was something to avoid, but read on for other reasons to stick with the original design.
2. Omission of the matching network brings on high harmonic content in both the motor waveform and on the wires leading to the motor, plus it increases the peak-to-peak amplitude of these two waveforms about 2.5 times. Note the time scale difference on the motor waveforms in Figure 31. A major frequency seen here is around 25KHz as opposed to the 42KHz of the other figures. If peak voltage across the motor is 50V, ~0.75A will flow in the motor. This means power loss and heating will be above optimum.
3. Using an undersized filter capacitor with the matching network results in wire and motor waveforms with higher than optimum amplitude and worse yet, they contain considerable high frequency energy (read this as a radiation problem).

12.0 CONCLUSION

While the typical PWM application is more involved (read this as more work) than the typical power op amp application, the additional steps required are in line with the additional power the PWM can deliver to the load. Using the tools and procedures presented here will bring out the best from the very compact and cost effective PWM amplifier. These tools are available free at www.apexmicrotech.com.

13.0 ADDENDUM-THE OP AMP INTEGRATOR

Any one for a slow comparator? That's what we find in Figure 35 (next page), where the feedback capacitor slows down the transition time. During the transition, the op amp is likely operating in a linear closed loop fashion. The input signal sets a current in R_{IN} because of the virtual ground property of the inverting input. With no current in or out of the op amp input pins, the input current path is through the feedback capacitor to the op amp output. Voltage is developed across a given capacitor, governed by the time and magnitude of the input. Linear operation ceases when the output of the op amp cannot meet the current requirement. This happens when the op amp slew rate, current capability or most often, voltage swing capability is exceeded. This is fine, the comparator has done its job of switching, with a controlled transition rate.

With a little modification, we can transform this switching circuit into a very useful linear tool. What is required is a form of feedback to maintain operation in the transition area, or the linear area. Figure 36 (next page) shows a generalized form of this idea where $f(x)$ is non-inverting. This function is often non-linear, but seldom contains step junctions.Confining our analysis to linear operation, there is no current in the op amp input pins. Looking at the summing junction with three connections, current in any given path must equal the sum of the other two paths. Therefore, capacitor current will be the algebraic sum of the input and feedback currents:

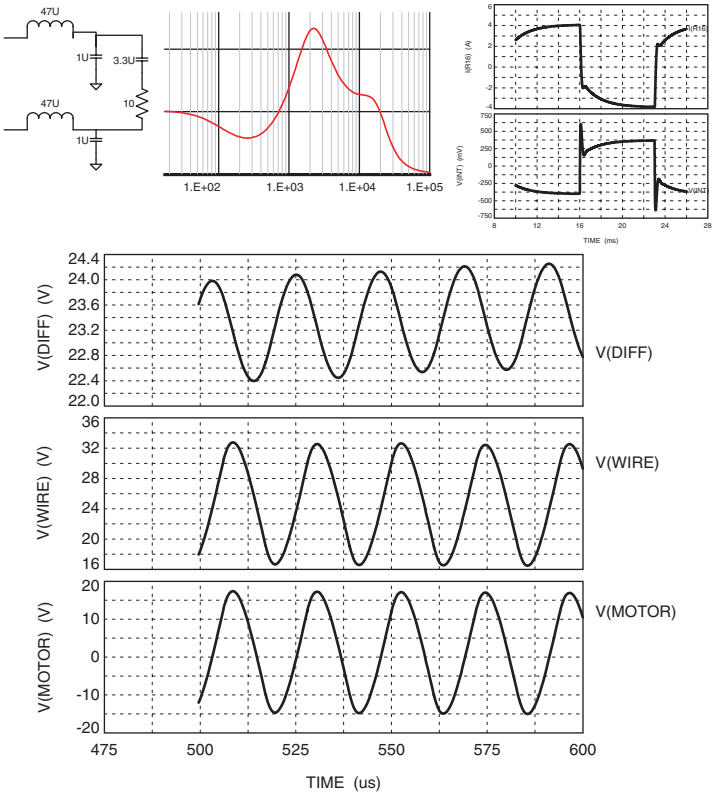


FIGURE 30. RESPONSE AND WAVEFORMS

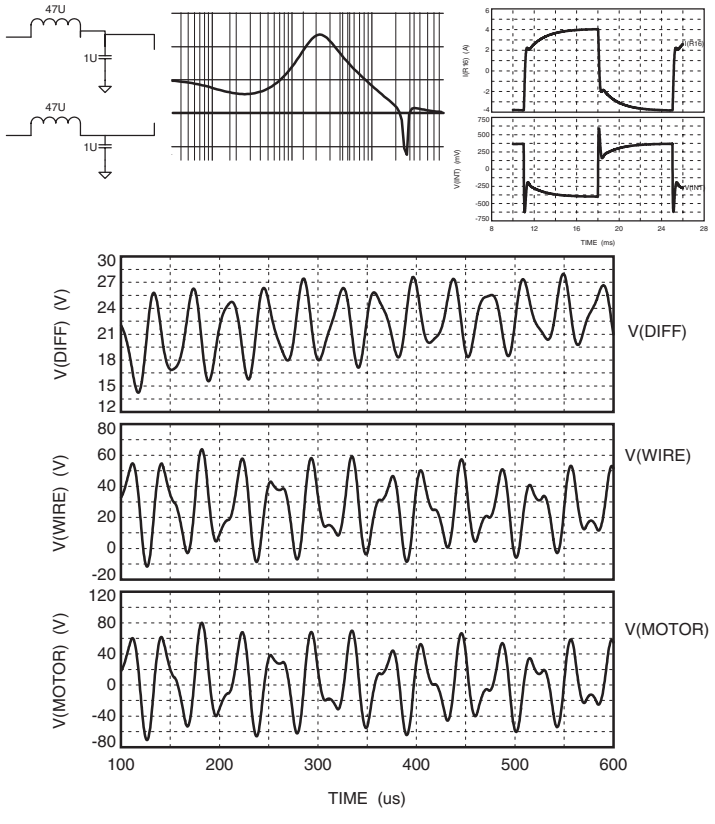


FIGURE 31. RESPONSE AND WAVEFORMS WITHOUT THE MATCHING NETWORK

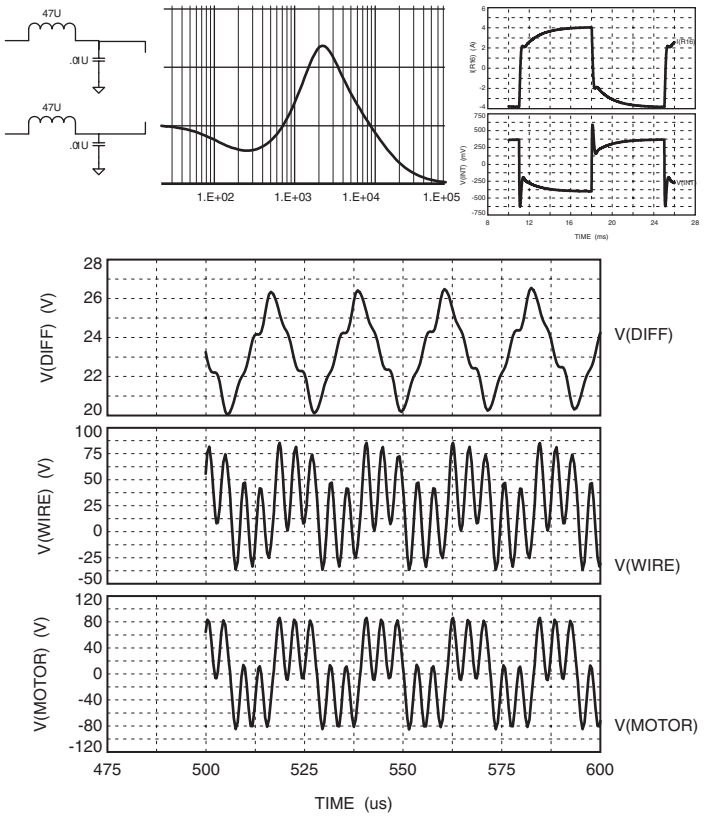


FIGURE 32. THE EFFECT OF SMALL CAPACITORS AND NO MATCHING NETWORK

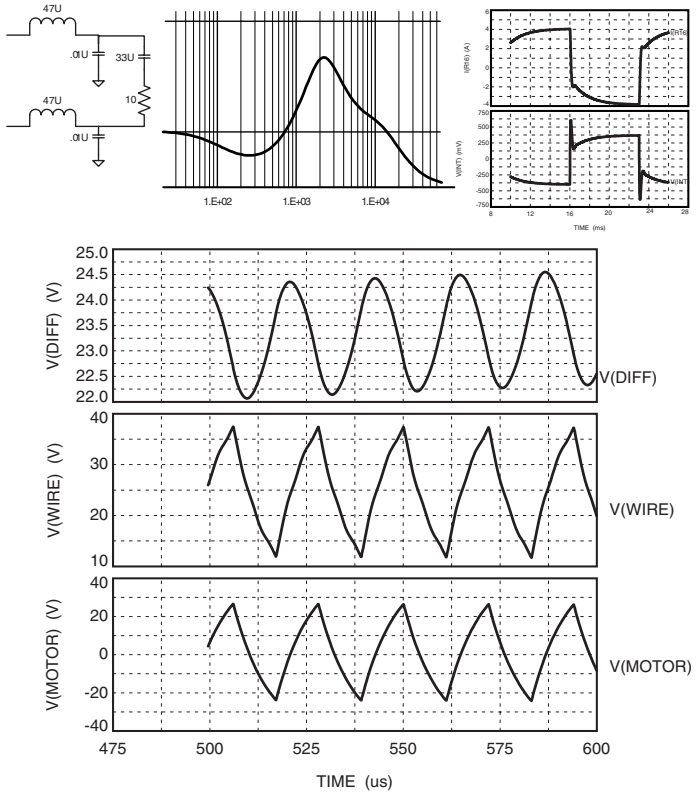


FIGURE 33. THE EFFECT OF SMALL CAPACITORS WITH THE MATCHING NETWORK

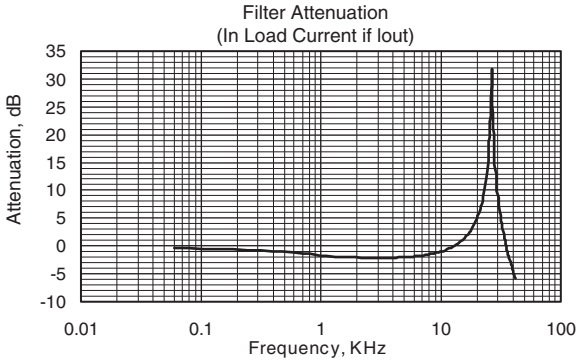


FIGURE 34. THE CAUSE OF THE FEEDBACK FACTOR DIP IN FIGURE 31

If I_{IN} and I_{FDBK} are equal and opposite, the output does not move.

Notice that our rule on movement of the output does NOT predict absolute level, only direction and rate of movement. This can be a magical elixir for many $f(x)$ functions. Assume a simple $f(x)$ of $V_{OUT} = V_{IN}$ - 3V as shown in Figure 37. Apply +1V as an input signal and mentally apply power. Start the analysis with the op amp output at zero, the non-powered state. The battery provides a -3V feedback signal, meaning 2mA will flow through the capacitor, causing the op amp to slew positive. Positive slew will continue, though at a decreasing rate, until input and feedback currents to the summing junction are equal and opposite. This condition will be reached when the $f(x)$ output = -1V and the op amp output = +2V.

That was simple and may not qualify as magic, but we get closer if we replace the battery with threshold voltage of a power MOSFET (moves around part to part and over temperature) and add a resistor to sense output current

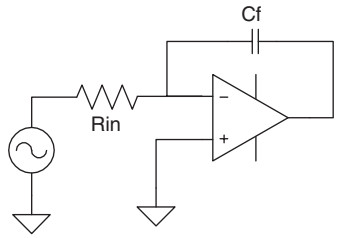


FIGURE 35. WHY WOULD ANYONE WANT A SLOW COMPARATOR?

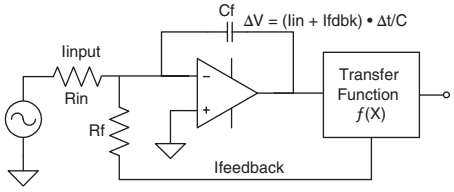


FIGURE 36. THE INTEGRATOR IN A SYSTEM

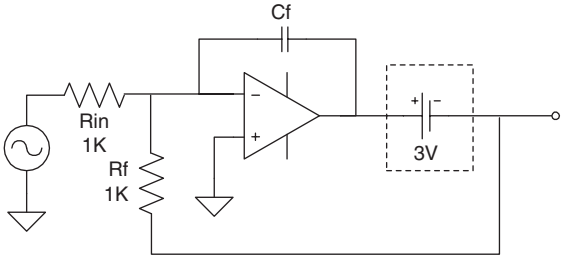


FIGURE 37. INCLUDING A SIMPLE TRANSFER FUNCTION

(which we may have very little control over). As long as our modifications of $f(x)$ do not take the circuit out of the linear operating range, the op amp still views its job as driving its output where ever needed to make the sum of all currents into the summing junction = zero.

Refer now to Figure 38 and assume the op amp output saturation is 3V from the rails, and common mode voltage is limited to 3V from the rails. Op amp output range is further

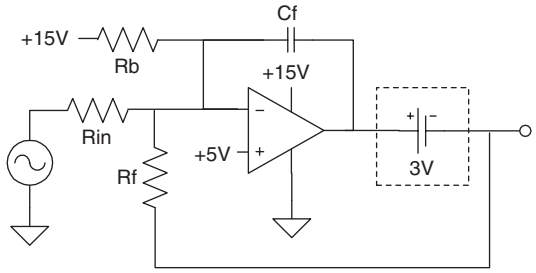


FIGURE 38. MOVING TO SINGLE SUPPLY OPERATION

that the input signal = ±5V (10Vp-p), R_{IN} = 1K, and our 15V supply is reference quality. Two resistors with a 2:1 ratio will yield a convenient 5V reference for the op amp +IN, giving a good safety margin on common mode voltage. Next, set overall gain according to $V_{OUTp\text{-}p}$ /$V_{INp\text{-}p}$.

$$R_F = R_{IN} * 9Vp\text{-}p / 10Vp\text{-}p = 900\Omega$$

Pick a convenient input voltage to compute the bias resistor needed to satisfy the requirement of zero net current to the summing junction. With the input signal = 5V, the circuit output will be zero (the overall transfer function = -0.9V/V). At this assumed point, current through R_{IN} = 0 and current through R_F = 5.556mA. We need 5.556mA bias from a reference of the opposite polarity of the feedback voltage with respect to the summing junction. This may seem a waste of words, but if $f(x)$ were +30V, the bias resistor would need to go to ground instead of the 15V reference.

$$R_{BIAS} = 10V / 5.556mA = 1.8K\Omega$$

If you care to check out operation at -5V input, current through R_{IN} = 10mA from a source negative with respect to the summing junction and current through R_{BIAS} = 5.556mA from a source positive with respect to the summing junction. For a net zero, current through R_F must be from a source positive (opposite that of the larger current) with respect to the summing junction and be equal to the difference of our first two currents. Start with the summing junction voltage and add I * R.

$$VOUT = 5V + (10mA - 5.556mA) * R_F = 9V$$

Basic operation of the circuit shown in side A of Figure 39 is identical to the common op amp four-resistor difference amplifier shown on the side B. Note that on the difference amplifier, the voltage difference between the output and Vref is always Vin (combined value) times the gain. Circuit A is doing the same thing, except the B output connection has been substituted for the reference input, meaning the voltage difference between the A output and B output is always Vin times the gain.

Next, assign circuit A input resistors of 1KΩ and feedback resistors of 10KΩ, providing an overall gain of 10, and a maximum supply voltage in the output stage of 50V. At 0V in, both outputs will be at 25V; at either input extreme, one output will move to 50V and the other will move to 0V. Assume the same op amp limitations and +15V supply as above. Starting with the non-inverting input, we know the pin needs to be pulled up at least 3V at all times; worst case is when the B output is 0V. The 1KΩ and the 10KΩ are effectively in parallel so we need enough current to pull 909Ω up to 3V or 3.3mA. With 12V across R_{BIAS}, its value should be 3.64KΩ. As this is a balanced circuit; the two bias resistors MUST be equal. A mismatch in these two resistors results in an offset.

Our last step is to check common mode voltage when the B output is 50V.

Many of us could quickly find a node voltage fed with two sources, through two resistors, but would be slowed down considerably when three legs feed the node. Refer to Figure 40 for a simple way to solve this circuit question with iteration. Start with the two legs having fixed voltage; find an equivalent voltage and resistance doing the same job as the original pair. V_{EQ} will be the voltage present if you removed the 10KΩ resistor, or 3.23V. R_{EQ} will be the parallel value of 3.64KΩ and 1KΩ, or 785Ω. The equivalent circuit for the +input can now be quickly used for any value of B output. With the B output = 50V,

$$V+IN = 46.77V / 10.785K\Omega * 785\Omega + 3.23V = 6.7V$$

This solution finds common mode voltage very safe with respect to the 12V specification on the upper end.

Congratulations! You have set up an integrator to drive a rudimentary stage average model of an SA60 running on Vcc = 15V (7.5V battery) and Vs = 50V (the 25V batteries).

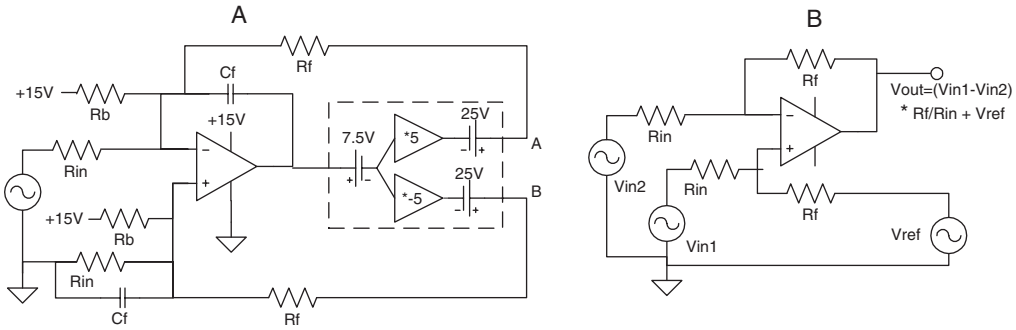


FIGURE 39. WHY WOULD ANYONE THINK UP THIS?

Biasing integrators for common mode voltage, or to level shift the input signal, is neither magic nor difficult. The overall transfer function must be known and linear operating limits must not be exceeded. The objective is then to reduce the sum of all currents to the summing junction to zero. When this is done, the charging rate of the capacitor is zero, and the op amp does not move. We have a stable operating point.

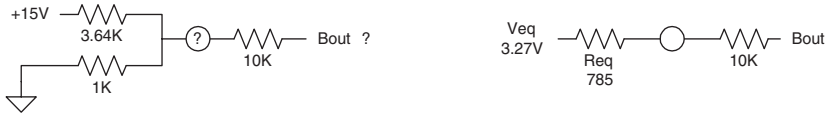


FIGURE 40. EQUIVALENT ELEMENTS HELP SOLVE FOR NODE VOLTAGE